

# Curriculum Vitae of Abelardo Jara-Berrocal

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## 1 AREAS OF INTEREST

Reconfigurable computing, HW/SW codesign, FPGA architecture, VLSI Design, VLSI CAD Tools Development.

## 2 EDUCATION

2005 PhD Student. College of Computer Engineering. University of Cincinnati, USA. VLSI Research Group. Courses taken up to date: GPA: 3.98, Doctoral Qualifying Examination passed in September 2006.

2002 Bachelor of Science in Electronics Engineering. Universidad Nacional de Ingenieria (UNI). Lima, Peru. 3rd best in the class (over 60 students)

## 3 RELEVANT GRADUATE COURSEWORK

Physical VLSI Design (Grade A), VLSI Design Automation (Grade A), VLSI Testing and Validation (Grade A), Compiler Theory and Lab (Grade A), Low Power VLSI (Grade A), VLSI Multi-technologies (Grade A), Digital Design Environments (Grade A), Automata Theory and Formal Languages (Grade: A), Computers Networking (Grade: A-), Silicon Programming (Grade A), Wireless and Mobyte Systems (Grade A), Design and Analysis of Algorithms (Grade A), Research on VLSI CAD Systems (Grade A).

## 4 TECHNICAL TRAINING

2004 Advanced International Course on VLSI Design Techniques. International Centre of Theoretical Physics (ICTP). Trieste, Italy. Certificate of merit of best student in the course.

2003 Advanced course in Rapid Digital Design using Xilinx FPGAs. International Centre of Theoretical Physics (ICTP). Trieste, Italy. Certificate of merit of best student in the course.

2003 Postgrades in Digital Communications and Computer Networking. National Institute of Research and Training in Telecommunications - (INICTEL). Lima, Peru

## 5 TECHNICAL SKILLS

- Programming languages: Java (Swing, JDBC), C++(STL Library, Crossplatform GUI development with wxWidgets), C (MPI), Bash Shell Scripting, VHDL, MATLAB (Simulink), SQL, Microsoft Visual Basic, HTML
- Programming tools: Netbeans, Code::Blocks, GNU Compiler and GNU Debugger, Visual C++
- Compiler generation tools: JLex, Java CUP.
- VLSI/CAD Tools: Magic Layout Editor, HSPICE, SPICE3, Synopsys Design Compiler, Synopsys Sirocco, IRSIM, HP Logic Analyzer 16500, PCB design with OrCAD Layout.
- FPGA Tools: Xilinx ISE, Xilinx EDK, Modelsim, Altera Quartus, Leonardo Spectrum.
- Operating Systems: Linux (Ubuntu), Solaris (SunOS), Windows 2000/NT/XP
- Document development with LaTeX.
- Networking: Configuration of Cisco routers (support for FXS Interfaces, VoIP, Diff-Serv, G.729, G.723, FRF12 encapsulation).

- DSP application development: Motorola 56811 DSP and Texas Instrument TMS320F240
- Office tools: Microsoft Word, Microsoft Excel, Microsoft Access and Microsoft Frontpage

## 6 REFEREED PUBLICATIONS

- Abelardo Jara Berrocal and Miguel Delgado, Finite Element Analysis Applied to the Solution of Electromagnetic Theory Problems. In Proceedings of IEEE International Congress INTERCON 99, Piura-Peru.
- Abelardo Jara Berrocal and Jorge Del Carpio, Design and implementation of a gamma camera acquisition board using a Xilinx FPGA. Tecnica Scientific Magazine 2003. Universidad Nacional de Ingenieria, Lima-Peru.
- Abelardo Jara Berrocal, Carlos Rodriguez, Jorge Del Carpio, Distributed arithmetic and Sigma Delta Modulation applied to Synthesis of FIR filters in FPGAs. In Proceedings of National Meeting of Peruvian Scientists (ECI-Peru), 2004.

## 7 COURSE PROJECTS

- Circuit Partitioner: Implemented a circuit partitioner using simulated annealing algorithm in C++. Certificate of merit of best program in the class.
- Placer and router: Implementation of a placer and router for VLSI using cluster growth floorplanning and grid routing.
- COOL Compiler: Developed a scanner, parser, and parts of semantic analyzer for the classroom object oriented language (COOL) using Jlex and Java CUP.
- A RISC microprocessor design: Designed a RISC microprocessor and modeled it in VHDL. Several benchmarks as FFT, sorter etc. are used to test the design.
- ASIC Design: Designed a north east (NE) router checker in Magic inside a fixed chip area. IR-SIM and HSpice were used for simulations. The fabricated chip was fabricated and tested using HP16500A Logic Analyzer.
- Digital Filter Design: Designed digital filters based on Hamming window, Blackman window and Hanning window using Matlab

## 8 RESEARCH EXPERIENCE

2005 Research and Development Center of National University of Engineering in Lima, Peru (CID-FIEE-UNI). Developed the hardware and software of a gamma camera Acquisition Board by request of the National Institute of Neoplastic Illnesses (INEN), Lima-Peru. The hardware was implemented using a Xilinx Spartan2E FPGA and the software using Visual C++. The digital part of the system was implemented using VHDL and Xilinx ISE and the PCB board was designed using OrCAD Layout.

2005 Electronics Engineering Department of the Peruvian Air Force (SELEC-FAP). Design and implementation of a digital acquisition system for the gyroscope of a Macci MB 339 aircraft using a Parvus PC 104 Space PC computer.

2004 Research and Development Center of National University of Engineering in Lima, Peru (CID-FIEE-UNI). Developed a FIR filter using Distributed Arithmetic in a Spartan3E FPGA. The filter took signals from a PCM 13-bit Motorola MC145483 audio codec. Development of the layout of the board using OrCAD.

2003 Research and Development Center of National University of Engineering in Lima, Peru (CID-FIEE-UNI). Development of a Matlab program to calculate the 2D stationary electric field in a microstrip line using variational finite elements method analysis.

## 9 TEACHING EXPERIENCE

2005 Teaching Assistant at the College of Computer Engineering of the University of Cincinnati: Physical VLSI (Fall 2006), VLSI Testing (Winter 2007), VLSI Multitech (Winter 2007), Computer Architecture (Fall 2006), Digital Systems (Spring 2006), Fundamentals of programming (Fall 2005), Control Theory (Winter 2006), Signals and Systems (Summer 2006).

2003-2004 Assistant Professor at the College of Electronics Engineering at the National University of Engineering in Lima, Peru in the courses of Digital Signal Processing Lab, Digital Systems and Electronic Circuits (Analog circuit design).

## 10 WORK EXPERIENCE

2005 Telefonica Empresas S.A.C., Lima-Per. Networking Engineer. Configuration and maintenance of Cisco routers and data communication equipments. .

2002-2004 National University of Engineering, Peru (April 2002 August 2005). Assistant professor.

2004 Electronic Service of the Peruvian Air Force (SELEC-FAP). Design engineer. Worked as a team member in the design and installation of a digital cockpit in a Macci MB339 aircraft using a Parvus PC 104 Space PC computer.

2003-2005 Technological Institute SISE, Peru (September 2003 August 2005). Professor of Visual C++, Java and Visual Basic.

2001 Computer Programmer at the Computer Center (UNI-CC) of the National University of Engineering in Lima, Peru.

## 11 LEADERSHIP EXPERIENCE

2006 Graduate Student Association ECECS University of Cincinnati, 2006 - Treasurer

1999 IEEE Student Branch Staff Member National University of Engineering, Peru, 1999 President of the Projects Committee

## 12 HONORS & AFFILIATIONS

2005-2007 University Graduate Scholarship, University of Cincinnati.

2005 Certificate of merit for best program in C++ using Simulated Annealing for solution of the bi-partitioning problem. VLSI Design Automation class, winter 2005. Computer Engineering College, University of Cincinnati.

2001-2003 Research Grant from the Office of Sponsored Research National University of Engineering, Peru, 2001-2003

2001 Second best student project award at the IEEE VIII International Conf. on Electrical, Electronics and Systems Engineering INTERCON, Peru, August 2001.

2001 Best student project award at the Peruvian National Congress of Students of Electrical and Electronics Engineering (CONEIMERA), Peru, November 2001.

2000-2001 University Grant for Computer Programmers of the Computer Center of the National University of Engineering (UNI-CC), Peru 2000-2001.

1997 Second best applicant to the National University of Engineering, Peru in the 1997 admission process.

## 13 INTERNATIONAL TESTS

GRE SCORE (March 2007): Quantitative (790) and Verbal (560)